

Patent Assignment Abstract of Title

Total Assignments: 1

Application #: 10086214 **Filing Dt:** 02/27/2002

Patent #: NONE

Issue Dt:

PCT #: NONE

Publication #: US20020138801 **Pub Dt:** 09/26/

Inventors: Laung-Terng Wang, Ming-Tung Chang, Shyh-Horng Lin, Hao-Jan Chao, Jaehee Lee, Hsin-Po Wang, Xiaoqing Wen, Po-Ching Hsu, Shih-Chia Kao, Meng-Chyi Lin, Sen-Wei Tsai, Chi-Chan Hsu

Title: Method and apparatus for diagnosing failures in an integrated circuit using design-for-debug (DFD) techniques

Assignment: 1

Reel/Frame: 012939/0774 **Received:** 06/04/2002 **Recorded:** 05/24/2002 **Mailed:** 07/31/2002 **Page:**

Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).

Assignors: WANG, LAUNG-TERNG (L.-T.)

Exec Dt: 04/23/2002

CHANG, MING-TUNG

Exec Dt: 04/18/2002

LIN, SHYH-HORNG

Exec Dt: 04/18/2002

CHAO, HAO-JAN

Exec Dt: 04/18/2002

LEE, JAEHEE

Exec Dt: 04/23/2002

WANG, HSIN-PO

Exec Dt: 04/22/2002

WEN, XIAOQING

Exec Dt: 04/23/2002

HSU, PO-CHING

Exec Dt: 04/22/2002

KAO, SHIH-CHIA

Exec Dt: 04/22/2002

LIN, MENG-CHYI

Exec Dt: 04/22/2002

TSAI, SEN-WEI

Exec Dt: 04/22/2002

HSU, CHI-CHAN

Exec Dt: 04/18/2002

Assignee: SYNTEST TECHNOLOGIES, INC.

SUITE 101

505 S. PASTORIA AVENUE

SUNNYVALE, CALIFORNIA 94086

Correspondent: LAW FIRM OF JIM ZEGER

JIM ZEGER

801 N. PITT STREET

#108

ALEXANDRIA, VA 22314

Search Results as of: 8/18/2004 3:40:02 P.M.

If you have any comments or questions concerning the data displayed, contact OPR / Assignments at 703-308-9723
Web interface last modified: Oct. 5, 2002